REMARKS / DISCUSSION OF ISSUES

Claim 1-3, 5-11 and 13-14 are pending in the application.

In the Final Office Action, claims 1-2, 5-9, 11 and 13-14 are rejected under 35 U.S.C. §112, second paragraph as allegedly indefinite. Without agreeing with the Examiner, and in the interest of advancing prosecution, claim 1 has been amended to remove the alleged informality noted by the Examiner. It is respectfully submitted that the rejection of claims 1-2, 5-9, 11 and 13-14 has been overcome and an indication as such is respectfully requested.

The Final Office Action rejects claims 1-3, 5-11 and 13-14 under 35 U.S.C. §103(a) over U.S. 6,990,570 (Masse) in view of U.S. 6,598,155 (Ganapathy) and U.S. 6,732,253 (Redford). It is respectfully submitted that claims 1-3, 5-11 and 13-14 are patentable over Masse, Ganapathy and Redford for at least the following reasons.

The rejected claims are patentable over Masse, Ganapathy and Redford at least because those references, taken individually or in combination, do not teach or suggest all the elements recited in independent claim 1, and similarly recited in independent claims 3 and 10, for example (illustrative emphasis provided):

> wherein **each functional unit has a private control unit** for controlling function of the each functional unit, including controlling a number of repetitions of execution of the function, and each functional unit is adapted to execute operations in an **autonomous** manner under control of the **private** control unit associated therewith so that access to an external instruction memory is reduced, including transfer of control to the control means upon completion of an operation included in the loop and execution of instructions of a subsequent loop instead of being stalled or executing a no-operation instruction, wherein each private control unit includes an instruction memory configured to hold one operation or a sequence of operations, and a counter indicating how often the one operation or the sequence of operations still has to be executed.

On page 5 of the Final Office Action, it is alleged that FIG 10, and column 11, lines 23-33 of Masse show "a counter indicating how often the one operation or the

sequence of operations still has to be executed," as recited in independent claims 1, 3 and 10. It is respectfully submitted that and column 11, lines 23-33 of Masse merely disclose the content of a loop counter register 922 represents the index count of a loop. This 'index count of the loop" (Masse, column 11, lines 25-26) does not indicate "how often the one operation or the sequence of operations still has to be executed," as recited in independent claims 1, 3 and 10.

Assuming, arguendo, that Masse does show this feature, it is still respectfully submitted that Masse, Ganapathy, Redford, and combinations thereof, do not teach or suggest "wherein each functional unit has a private control unit for controlling function of the each functional unit, including controlling a number of repetitions of execution of the function, and each functional unit is adapted to execute operations in an autonomous manner under control of the private control unit associated therewith," as recited in independent claim 1, and similarly recited in independent claims 3 and 10.

On page 6 of the Final Office Action, first two full paragraphs, it is correctly noted that this feature is not taught or suggested by Masse and Ganapathy. FIG 1 and column 2, lines 61-65 of Redford are cited in an attempt to remedy the deficiencies in Masse and Ganapathy.

It is still respectfully submitted that column 2, lines 61-65 line10 of Redford specifically recite:

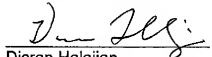
> Referring to FIG. 1, a **single** instruction multiple datapath (SIMD) processor 10 includes an instruction cache 12, control logic 14, a serial datapath, and a number of parallel datapaths labeled 18a, 18b, 18c, 18, . . . 18n. The parallel datapaths 18 write to a memory 20. Each of the datapaths 18 has an associated **processor enable (PE) bit 22**. (Emphasis added)

Thus, Redford discloses a **single** processor 10 that includes parallel datapaths 18 to write to a memory 20, once a datapath 18 is enabled by a processor enable (PE) **bit** 22. That is, the do not have their own private control units. Rather, the Redford datapaths 18 are controlled by a single processor 10. Accordingly, it is respectfully submitted that independent claims 1, 3 and 10 are allowable. In

addition, it is respectfully submitted that claims 2, 5-9, 11 and 13-14 are allowable at least because they depend from independent claims 1 and 10, as well as for the separately patentable elements contained in each of the dependent claims.

In view of the foregoing, applicant(s) respectfully request(s) that the Examiner withdraw the objection(s) and/or rejection(s) of record, allow all the pending claims, and find the application to be in condition for allowance. If any points remain in issue that may best be resolved through a personal or telephonic interview, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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